REMARKS

Claims 1, 2, and 4-10 are pending in the application. All claims stand rejected under 35 U.S.C. §102(b) as allegedly being anticipated by U.S. Patent No. 5,528,177 ("Sridhar"). Claim 10 is being added.

The Examiner maintains that Sridhar teaches all claimed features in FIG. 2g. Applicants respectfully disagree. Contrary to the position, initially taken in the Office Action mailed on March 29, 2002 and maintained throughout the prosecution of this application by the Examiner, The Sridhar circuit in FIG. 2g **requires** the inverter 232 to provide the same OR output as that provided by the inventive three-transistor circuit shown in FIG. 2A of the application. It is the advantage of the present invention over prior art to in that achieve the OR operation, only three transistors are used reducing the number of components thereby and reducing the delay.

The output, of the inventive three-transistor circuit without the use of the inverter, with different input values provided, is shown in a table in FIG. 2B of the present application. The table shows the following values:

A	B	~B	A+B
0	0	1	**0**
1	0	1	**1**
0	1	0	**1**
1	1	0	**1**

The OR output signal can be used directly from the transmission gate, no inversion circuitry is **required** to produce OR output, with static complementary metal oxide semiconductor (CMOS) complex logic gates, such as a NAND circuit, to perform more complex functions using fewer transistors with faster delays while utilizing less power.

The same output values table constructed for Sridhar is

A	B	~B	A+B
0	0	1	**1**
1	0	1	**0**
0	1	0	**0**
1	1	0	**0**

The difference is caused by the Sridhar requirement of an output inverter 232 to create an

output signal indicative of an OR operation performed on the first and second input signals. Most of the Sridhar circuits require inverters. Therefore, Sridhar does not teach or describe "providing an output to be combined with said intermediate signal to create an output signal indicative of an OR operation performed on said first and second input signals, said output signal is output from the MOSFET logic circuit to any static CMOS logic gate" claimed in amended Claim 1.

For at least the reasons discussed herein, Sridhar does not disclose, teach, or suggest the MOSFET logic circuit for performing OR operation recited in Claim 1. It is respectfully submitted that Claim 1, as amended, is patentable over Sridhar. By virtue of their dependence upon Claim 1, it is further submitted that Claims 2, 4-9 are also patentable over Sridhar et al. New Claim 10 was added to more narrowly claim limitations of Claim 1. Claim 10, therefore is also patentable.

In view of the foregoing amendments and remarks, it is respectfully submitted that this case, and all pending claims, are in condition for allowance. Such early and favorable action is earnestly solicited.

Should the Examiner have any questions concerning this communication or feel that an interview would be helpful, the Examiner is requested to call the undersigned at the number indicated below.

Respectfully submitted,

Paul J. Farrell
Reg. No. 33,494
Attorney for Applicants

DILWORTH & BARRESE, LLP
333 Earle Ovington Blvd.
Uniondale, New York 11553
(516) 228-8484